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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,813	09/17/2003	Junichi Nakamura	117212	4050

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EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,813	NAKAMURA, JUNICHI	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-12,14 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-12,14 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed on 23 March 2006 in this application after final rejection (mailed 23 December 2005). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's 'Amendment' filed 23 March 2006 has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 4-10, 12, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Sato et al (US 5,712,652 A) [which was originally listed on the 'Notice of References Cited' mailed 28 June 2005].

Regarding claim 1, Sato discloses an optoelectronic-device substrate [Fig. 4; 301], comprising: a common electrode [Fig. 1; 12] applied with a fixed potential (see Fig. 5; Column 9; Lines 62-64); a pixel electrode [Fig. 1; 3]; a storage unit [Fig. 1; 100] for storing pixel data [Fig. 1; video signals transmitted through data lines 1-na and 1-nb, displaying black on a normally white display] (see Column 24, Lines 46-56); a phase-inversion circuit [Fig. 1; 15] that outputs a phase-inversion signal [Fig. 1; AC drive signal through line 8-n] for inverting a phase of pixel data from the storage unit (see Column 9, Lines 28-61); a first switch [Fig. 1; 9] for generating a data-inversion signal [Fig. 1; output of first transfer gate 9], based on the phase-inversion signal, the data inversion signal being a signal that inverts signal phase of display data between a positive potential [Fig. 5; +Vo] and a negative potential [Fig. 5; -Vo]; and a second switch [Fig. 1; 11] for switching between the data-inversion signal from the first switch and a zero-data signal [Fig. 1; reset signal through line 10] that indicates that a potential equivalent to the fixed potential applied to the common electrode should be applied to the pixel electrode (see Column 12, Lines 1-20), the second switch selecting the data-inversion signal when pixel data is stored in the storage unit [Fig. 1; transfer gate 9 is selectively turned on by the presence of black pixel data], and the zero-data signal when the pixel data is not stored in the storage unit [Fig. 1; transfer gate 11 is selectively turned on by the absence of black pixel data], the selected one of the data-inversion signal and the zero-data signal being transmitted to the pixel electrode (see Column 24, Lines 46-56).

Regarding claim 4, Sato discloses the storage unit being formed as an SRAM [Fig. 1; 4-7] (see Column 9, Lines 28-61).

Regarding claim 5, Sato discloses the memory-cell array including: a plurality of first signal lines [Fig. 1; 2-n] to connect one group of address terminals [Fig. 1; 6 & 7 gates] included in one group of the storage units in parallel, the one group of the storage units being provided along a row direction; a plurality of second signal lines [Fig. 1; 1-na and 1-nb] to connect one group of data terminals [Fig. 1; 6 & 7 sources] included in one group of the storage units in parallel, the one group of the storage units being provided along a column direction; and a plurality of third signal lines [Fig. 1; 8-n] to connect one group of phase-inversion terminals [Fig. 1; transfer gate 9 input] included in one group of the storage units in parallel, the one group of the storage units being provided along the row direction or the column direction; and the optoelectronic-device substrate further including: a first driver circuit [Fig. 1; 15] to transmit address signals in sequence to the storage units via the plurality of first signal lines, the storage units being provided along the row direction; a second driver circuit [Fig. 1; 14] to transmit the pixel data to the storage units at one time via the plurality of second signal lines, the storage units being provided along the column direction; and a third driver circuit [Fig. 1; 15] to transmit phase-inversion signals to each group of the storage units via the plurality of third signal lines, the group of the storage units being provided along the row direction or the column direction (see Column 9, Lines 28-67).

Regarding claim 6, Sato discloses the third driver circuit having a phase-inversion circuit [Fig. 2; 205a and 205b] to invert the phase of the pixel data, and the phase-inversion circuit

inverting the phase of the pixel data before the pixel data is transmitted to the storage units (see Column 12, Line 61 - Column 13, Line 7).

Regarding claim 7, Sato discloses the memory-cell array including: a plurality of first signal lines [Fig. 1; 2-n] to connect one group of address terminals [Fig. 1; 6 & 7 gates] included in one group of the storage units in parallel, the one group of the storage units being provided along a row direction; a plurality of second signal lines [Fig. 1; 1-na and 1-nb] to connect one group of data terminals [Fig. 1; 6 & 7 sources] included in one group of the storage units in parallel, the one group of the storage units being provided along a column direction; and a plurality of third signal lines [Fig. 1; 8-n] to connect one group of phase-inversion terminals [Fig. 1; transfer gate 9 input] included in one group of the storage units in parallel, the one group of the storage units being provided along the row direction or the column direction; and wherein the optoelectronic-device substrate further including: a row-address-decoder driver circuit [Fig. 1; 15] to transmit row-address data for selecting any of rows of the storage units via the plurality of first signal lines, the storage units being provided along the row direction; a column-address-decoder driver circuit [Fig. 1; 14] to transmit column-address data to select any of columns of the storage units via the plurality of second signal lines, the storage units being provided along the column direction, and the pixel data output to the storage units designated by the row-address data and the column-address data; and a phase-inversion driver circuit [Fig. 1; 15] to transmit a phase-inversion signal to each group of the storage units via the plurality of third signal lines, each group of the storage units being provided along the row direction or the column direction (see Column 9, Lines 28-67).

Regarding claim 8, Sato discloses the phase-inversion driver circuit having a phase-inversion circuit [Fig. 2; 205a and 205b] to invert the phase of the pixel data, the phase-inversion circuit inverting the phase of the pixel data in a predetermined cycle [i.e. 60Hz frame writing frequency] regardless of the number of the storage units whose display information is rewritten according to the pixel data (see Column 13, Lines 3-33).

Regarding claim 9, Sato discloses a digitally-driven liquid-crystal display, comprising the optoelectronic-device substrate [Fig. 4; 301]; a counter substrate [Fig. 4; 312]; a liquid crystal layer [Fig. 4; 315] provided between the optoelectronic device substrate and the counter substrate (see Column 10, Line 64 - Column 11, Line 14); and a common electrode [Fig. 4; 12] to supply a voltage having a potential that is equivalent to the potential of zero data transmitted to the optoelectronic-device substrate (see Fig. 5; Column 12; Lines 6-19).

Regarding claim 10, Sato discloses an electronic apparatus, comprising the digitally driven liquid crystal display; and a display unit to display an image through the digitally-driven liquid-crystal display (see Column 1, Lines 5-10).

Regarding claim 12, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, Sato discloses a method of driving an optoelectronic-device substrate [Fig. 4; 301] that includes a memory-cell array [Fig. 1; 100] including a plurality of storage units that is arranged in matrix form along a row direction and a column direction and that is digitally driven,

and a pixel electrode [Fig. 1; 3] to retrieve pixel data [Fig. 1; video signals transmitted through data lines 1-na and 1-nb, displaying black on a normally white display] (see Column 24, Lines 46-56) stored in the storage units as an electrical signal [Fig. 1; AC drive signal through line 8-n] (see Column 9, Lines 28-61), the method comprising: performing at least one of inverting [Fig. 2; via 205a and 205b] the phase of the pixel data before the pixel data is transmitted to the storage units, and inverting [Fig. 1; via AC drive signals applied to transfer gate 9] the phase of the pixel data after the pixel data is transmitted to the storage units (see Column 11, Line 49 - Column 12, Line 46).

Regarding claim 14, Sato discloses the performing including selecting the storage units provided along the row direction in sequence, and inverting the phase of the pixel data at the same time (see Column 12, Lines 20-29).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al (US 5,712,652 A) in view of Ichikawa et al (US 6,559,821 B2).

Regarding claim 11, Sato discloses a control circuit [Fig. 2; 206] (see Column 13, Lines 8-22) to control the digitally-driven reflection-type liquid crystal display (see Fig. 4; Column 23,

Lines 40-49). Sato does not expressly disclose a projector-lens system and light-source to magnify and project an image of the reflection-type liquid crystal display.

However, Ichikawa does disclose a light-source unit [Fig. 13; 371] to supply projection light; and a projector-lens system [Fig. 15A; 380] to magnify and project an image of a reflection-type liquid crystal display [Fig. 13; 378] (see Column 16, Lines 1-34).

Sato and Ichikawa are analogous art, because they are from the shared field of reflection-type liquid crystal display devices. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to combine Sato's optoelectronic device with Ichikawa's light-source and projector-lens system, replacing Ichikawa's reflection-type liquid crystal display with Sato's reflection-type liquid crystal display, so as to avoid the high costs associated with manufacturing a large liquid crystal display screen by instead optically enlarging the displayed image of a relatively small LCD screen (see Ichikawa: Column 1, Lines 23-36).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al (US 5,712,652 A) in view of Adachi et al (US 6,924,824 B2).

Regarding claim 15, Sato discloses the performing including transmitting a cycle [i.e. an ordinary 60Hz frame writing frequency] with which the phase-inversion signal to the storage units is provided along the row direction, and making a cycle with which pixel data is transmitted to the storage units provided along the row direction variable [i.e. a frequency lower than the ordinary frame writing frequency] so that the cycles can change in synchronization (see Column 13, Lines 23-33). Sato does not expressly disclose making a cycle of sub-frames variable so as to present gray scale.

However, Adachi does disclose making a cycle of sub-frames variable [Fig. 15; SF1-SF4] so as to present gray scale [Fig. 15; Gray Scale 0-15] on a digitally driven [Fig. 15; VH & VL] liquid crystal display device [Fig. 14; 101] (see Column 4, Lines 15-40).

Sato and Adachi are analogous art, because they are from the shared field of digitally driving liquid crystal display devices. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to drive Sato's liquid crystal display with Adachi's variable sub-frame driving method, so as to display an improved gray scale image while minimizing potential power loss (see Adachi: Column 3, Lines 49-59).

Response to Arguments

8. Applicant's arguments (see page 7 of the 'Amendment' filed 23 March 2006) with respect to claims 1, 4-12, 14, and 15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The applicant is hereby notified that the examiner's art unit has recently changed from Art Unit 2673 to Art Unit 2629, please direct all future correspondence accordingly. Thank you.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J.P.
12 April 2006